Broadband RF Power Amplifier Design Methodology Using Sequential Harmonic Characterization

by

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A THESIS

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Abstract

Radio Frequency Power Amplifier (RFPA) amplifies the communication signals to the required power level for transmission. It is the most power consuming stage in a transceiver chain; consequently, any improvement in terms of dissipated power and efficiency of the power amplifier affects the overall power budget of the transmitter. Also, efficient performance of the RF power amplifier over extended ranges of frequency is one of the most challenging areas in implementing multi-band transmitter systems. In this thesis, a design methodology for multi-octave RF power amplifiers is presented based on the proposed sequential harmonic characterization. Compared to the conventional method, a more optimal performance is achieved using the proposed technique. To validate the proposed method, a broadband multi-octave power amplifier prototype was designed and fabricated using a Cree GaN HEMT device that exhibits drain efficiency of 53% - 64% across 0.7 – 4.0 GHz corresponding to the fractional bandwidth of 140%.
Acknowledgements

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Finally, I would like to express my love and thanks to my parents who devoted their life for their children.
To my parents for their endless love and support
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<td>ADS</td>
<td>Advanced Design Systems</td>
</tr>
<tr>
<td>BS</td>
<td>Base Station</td>
</tr>
<tr>
<td>BTS</td>
<td>Base Transceivers Station</td>
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<tr>
<td>CAD</td>
<td>Computer Aided Design</td>
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<td>CDMA</td>
<td>Code Division Multiple Access</td>
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<tr>
<td>CMPR</td>
<td>Compression</td>
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<td>CR</td>
<td>Cognitive Radio</td>
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<tr>
<td>DUT</td>
<td>Device Under Test</td>
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<tr>
<td>EB</td>
<td>exabyte ($10^{18}$B)</td>
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<tr>
<td>EDGE</td>
<td>Enhanced Data-rates for Global Evolution</td>
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<tr>
<td>ESR</td>
<td>Equivalent Series Resistance</td>
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<tr>
<td>FDD</td>
<td>Frequency Division Duplex</td>
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<td>GaN</td>
<td>Gallium Nitride</td>
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<td>GaAs</td>
<td>Gallium Arsenide</td>
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<tr>
<td>GPIB</td>
<td>General Purpose Interface Bus</td>
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<tr>
<td>HB</td>
<td>Harmonic Balance</td>
</tr>
<tr>
<td>HEMT</td>
<td>High Electron Mobility Transistor</td>
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<tr>
<td>ICT</td>
<td>Information &amp; Communication Technology</td>
</tr>
<tr>
<td>JTRS</td>
<td>Joint Tactical Radio System</td>
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<tr>
<td>LTE</td>
<td>Long Term Evolution</td>
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<tr>
<td>MAN</td>
<td>Metro Area Network</td>
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<tr>
<td>MMIC</td>
<td>Monolithic Microwave Integrated Circuit</td>
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<tr>
<td>OFDM</td>
<td>Orthogonal Frequency Division Multiplexing</td>
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<td>PA</td>
<td>Power Amplifier</td>
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<tr>
<td>PAE</td>
<td>Power Added Efficiency</td>
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<tr>
<td>PAN</td>
<td>Personal Area Network</td>
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<tr>
<td>PAPR</td>
<td>Peak to Average Power Ratio</td>
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<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
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<td>PMR</td>
<td>Public Mobile Radios</td>
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<td>RF</td>
<td>Radio Frequency</td>
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<tr>
<td>SDR</td>
<td>Software Defined Radio</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
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<tr>
<td>SRF</td>
<td>Self Resonance Frequency</td>
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<tr>
<td>WCDMA</td>
<td>Wideband Code Division Multiple Access</td>
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<tr>
<td>VHF</td>
<td>Very High Frequency</td>
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<tr>
<td>WiMAX</td>
<td>Worldwide Interoperability for Microwave Access</td>
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<tr>
<td>WLAN</td>
<td>Wireless Local Area Network</td>
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Chapter 1

Introduction

1.1 Motivation

Communication services have experienced unprecedented growth in the last few decades. Data rates of wireless networks, as one of the largest parts of Information and Communication Technology (ICT) systems, have been rising by a factor of 10 every five years [1]. In addition to non-smart phones and laptops, the recent widespread use of smart phones, tablets, and online social network, cellular data traffic continues to increase significantly. Monthly traffic of global mobile data was reported as 2.8 EB (Exabytes=10^{18}B) in 2014 and is estimated to be 11.2 EB by 2017 [2]. Average monthly traffic per smart phone in 2011 was reported as 150 MB and is estimated to increase to more than 2500 MB by 2016.

Such an expanding volume of data traffic comes with the cost of increasing energy consumption. Currently, ICT infrastructures consume 3% of world-wide energy corresponding to 2% of world-wide CO_2 emissions [3]. In particular, mobile wireless networks consume approximately 120 TWh of electricity per year, which is equivalent to the amount of power produced by more than 14 average-sized American nuclear power plants. This amount

![Figure 1.1](image)

**Figure 1.1:** (a) Breakdown of power consumption in a typical cellular network (b) Power consumption distribution in base stations [5]
of energy consumption corresponds to approximately 72 million tons of CO$_2$ emissions per year, which is equivalent to annual greenhouse gas emissions produced by 14 million cars [4]. If energy consumption of ICT systems continues to increase at the present pace, “green” policies necessitate energy efficient approaches.

Fig.1.1(a) shows a breakdown of power consumption in a typical cellular network. As it can be seen, more than 50% of power is consumed in base station (BS) equipment [5]. Due to increasing density of wireless networks, the number of cellular BSs operating worldwide in 2020 is estimated to reach 50 million [6]. This provides insight into critical areas of research and development for reducing energy consumption in wireless communications.

The typical block diagram of a base transceiver station (BTS) is shown in Fig.1.2, including transmitter and receiver chains [7]. As depicted in Fig.1.1(b), a large portion of the power is consumed by the power amplifier in the wireless transmitter system. The power amplifier is employed to amplify signals for transmission. Consequently, efficiency enhancement of the power amplifier has a significant impact in the overall reduction of the power consumption in mobile base stations and wireless networks accordingly.

**Figure 1.2:** Mobile base station diagram [7]
Furthermore, with the substantial growth of wireless technology, multiple communication standards have been developed to adapt to various applications. Recent advances in wireless communications have enabled radio systems to use spectrum more efficiently than in the past [8]. Cognitive Radio (CR) and Software Defined Radio (SDR) architectures have been considered promising technologies for exploiting spectrum in a wide range of frequency from hundreds of MHz to several GHz covering multiple mobile communication standards.

These architectures offer coexistence of the various wireless networks, i.e., cellular, wireless Personal Area Network (PAN), wireless Local Area Network (WLAN), and wireless Metro Area Network (MAN) [9] as depicted in Fig.1.3 [10]. Such coexistence of services and standards takes place on one platform. SDRs have a wide range of applications such as cellular BTSs for commercial use, Public Mobile Radios (PMR) used by law enforcement personnel and emergency responders, and Joint Tactical Radio System (JTRS) for military communications [11].

The difference between SDR and conventional transceivers is that operation frequency and modulation format are determined by software. Indeed, the major enablers of such
configurations are wide-band front-end components, particularly power amplifiers. Using a single wide-band PA instead of several narrow band PAs reduces overall costs effectively due to the elimination of further PAs circuitry including bias, matching networks, filters and overall size shrinking.

Broadband performance will then become another key aspect of the power amplifier design in addition to efficiency. Consequently, efficient performance of RF power amplifier over extended range of frequency is of particularly high importance.

1.2 Objectives of the Thesis

The main objective of this thesis is to give an optimal design procedure for designing multi-octave RF power amplifiers for the broadband wireless transmitter systems Software Defined Radio and Cognitive Radio applications, based on the proposed sequential harmonic characterization technique. The following steps are taken to reach the main objective:

1. Study the basic concept of power dissipation and efficiency in the PA and the importance of harmonic load impedances toward high efficiency PA design.
2. Review high efficiency and wide-band PA design approaches.
3. Identify the impact of in-band harmonic load impedances for multi-octave design.
4. Propose a design methodology for exploiting in-band harmonic effectively to achieve optimum performance.
5. Design, simulation and implementation of a broadband high efficiency RF power amplifier based on the proposed methodology.

1.3 Thesis layout

The need of high efficiency and wide-band power amplifier design described in the first chapter is followed in Chapter 2 with a review of high efficiency and wide-band power amplifier design techniques. Experimental works reported in the literature are studied in terms of theoretical and practical design challenges. These approaches are divided into
two main categories: waveform engineering based approaches and device characterization based techniques. Starting with classic high efficiency designs, wide-band PA design based on waveform manipulation is examined. Considering the advantages and limitations, the wide-band design technique based on device characterization using load-pull is studied. Then, multi-octave design, as the next step of wide-band PA design, is studied in terms of harmonic characterization.

Based on these studies, sequential harmonic characterization as a broadband design methodology for multi-octave RF power amplifier is presented in Chapter 3. The performance of this method is verified through PA design and simulation in ADS using a Cree GaN HEMT device model. Active device characterization is carried out using sequential characterization compared with conventional load-pull for a multi-octave targeted bandwidth. Simulation and experimental results demonstrate broadband performance in a good agreement with presented method.

Finally, Chapter 4 summarizes the motivation and contribution of this work towards wide-band RFPA design and outlines further steps for future works.
Chapter 2

High Efficiency and Wide-band Power Amplifier Design Approaches

2.1 Introduction

Design of power amplifier deals with different requirements. High power gain and output power levels lead to an increase in the number of amplifier stages, thus increasing the overall size. Also, power amplifier is the most power consuming stage in a transceiver chain, such that any improvement in terms of dissipated power and efficiency affects the overall performance of the system [12].

A high efficiency design means that more DC supplied power converted to the RF transmitted power resulting in less dissipated power in the active device. Then, less heat will be generated resulting in longer lifetime of circuit components. In other words, a high efficiency design is required to optimize and mitigate the thermal management, due to reduced power dissipation in the active device. Also, in order to enable the transmitter to work in different frequency bands and different standard, it is needed to have high efficiency in a large frequency band, which is hard to achieve. In this chapter, the impact harmonic components on the efficiency of the PA is first studied. Next, the high efficiency and wide-band PA design techniques are reviewed in two main categories of the waveform engineering and load-pull approaches.

2.2 Harmonic Tuning in PA design

A high efficiency design implies delivering a significant amount of output power at a fundamental frequency, while having power dissipated as little as possible in the active device. High efficiency design approaches are based on waveform analysis of the active device where the overlap between the voltage and current waveforms is minimized. Then power dissipation is reduced in the active device and efficiency is improved. The effect of harmonic components of the drain voltage and current on the minimized overlap is the key
Figure 2.1: Simple schematic of the power amplifier

aspect of a high efficiency design. Recognizing the fundamental mechanism of the power transfer and the amplifying process through the active device is important to understand the role harmonics play. A basic and simple configuration of a power amplifier is shown in Fig.2.1. $L_{RFC}$ is Radio Frequency Choke (RFC) inductance which is ideally DC short-circuited and RF open-circuit. RFC can be considered as a current source that sustains both positive and negative voltages, then allowing drain voltage to swing up to $2V_{DD}$. $C_{RFC}$ is a DC-blocking capacitor which is ideally DC open-circuit and RF short-circuited.

Driven by an external RF source, the active device receives DC power from supply and delivers output RF power to the load at a fundamental frequency. The power conversion mechanism is described by the drain efficiency using the Eq.2.1:

$$\eta = \frac{P_{out,f}}{P_{DC}}$$

(2.1)

where $P_{out,f}$ is output power delivered to the load at fundamental frequency and $P_{DC}$ is DC power provided by the power supply. The maximum theoretical efficiency of 100% means that DC power is completely delivered to the load at the fundamental frequency. The DC
power is converted to three different terms as below [13]:

\[ P_{DC} = P_{diss} + P_{out,f} + \sum_{n=2}^{\infty} P_{out,nf} \]  \hspace{1cm} (2.2)

where \( P_{diss} \) is dissipated power in the transistor, \( P_{out,f} \) is output power delivered to the load at fundamental frequency, and \( P_{out,nf} \) is the output power in harmonic frequencies. Theoretically, maximum efficiency is achieved when dissipated power and output power at harmonic frequencies are minimized. Dissipated power can be expressed as:

\[ P_{diss} = \int_T v_{DS}(t) \cdot i_D(t) dt \]  \hspace{1cm} (2.3)

Eq. 2.2 shows that non-overlapping drain waveforms are necessary but not sufficient for maximum efficiency. The other term that guarantees maximum theoretical efficiency is output power at harmonic frequencies which was not accurately addressed in classic harmonically tuned power amplifiers where all harmonics were shorted. Fig. 2.2 shows the degradation of efficiency when only the overlapping condition is observed and output power at harmonic frequencies is not considered.

As it can be seen, both drain voltage and drain current are hypothetically assumed square wave with zero overlapping. Since drain waveforms are square waves, they consist
only of odd harmonics. Recall following integrals:

\[
\int_{-\pi}^{\pi} \cos n\theta \cos m\theta d\theta = \int_{-\pi}^{\pi} \sin n\theta \sin m\theta d\theta = \begin{cases} 
0 & n \neq m \\
\pi & n = m
\end{cases} \tag{2.4}
\]

\[
\int_{-\pi}^{\pi} \sin n\theta \cos m\theta d\theta = 0 \text{ for all values of } m \tag{2.5}
\]

Using Fourier series analysis, drain voltage and current waveforms of Fig.2.2(a) can be expressed as:

\[
i_D(\theta) = \frac{I_{\text{max}}}{2} + \frac{2I_{\text{max}}}{\pi} \sin(\theta) + \frac{2I_{\text{max}}}{3\pi} \sin(3\theta) + \frac{2I_{\text{max}}}{5\pi} \sin(5\theta) + \ldots \tag{2.6}
\]

\[
v_D(\theta) = \frac{V_{\text{max}}}{2} - \frac{2V_{\text{max}}}{\pi} \sin(\theta) - \frac{2V_{\text{max}}}{3\pi} \sin(3\theta) - \frac{2V_{\text{max}}}{5\pi} \sin(5\theta) - \ldots \tag{2.7}
\]

where \(\theta = \omega t\) and \(\omega = 2\pi f\). Therefore, for dissipated power we have:

\[
P_{\text{diss}} = \int v_{DS}(\theta).i_D(\theta)d\theta = \int [\frac{I_{\text{max}}}{2} \times \frac{V_{\text{max}}}{2} - \frac{2I_{\text{max}}}{3\pi} \sin(3\theta) \times \frac{2V_{\text{max}}}{3\pi} \sin(3\theta) - \ldots]d\theta = 0 \tag{2.8}
\]

Since drain waveforms of Fig.2.2(a) are non-over lapped, the dissipated power is zero. However, the harmonic terms are not zero resulting in output power at harmonic frequencies and almost 20% of degradation in maximum theoretical efficiency of 100% as below:

\[
\eta = \frac{P_{\text{out},f}}{P_{\text{DC}}} = \frac{\frac{1}{2} V_{ds,f} \times I_{d,f}}{\frac{1}{2} V_{DC} \times I_{DC}} = \frac{\frac{1}{2} \left[ \frac{2(I_{\text{max}})}{\pi} \right] \times \left[ \frac{4}{\pi} V_{DD} \right]}{(I_{\text{max}}/2) \times V_{DD}} = \frac{8}{\pi^2} \approx 81\% \tag{2.9}
\]

Such degradation of efficiency can be alleviated if the product of harmonic terms is somehow zero. Harmonically tuned amplifiers based on waveform engineering exploits odd
and even harmonics effectively such that output power at harmonics is theoretically zero, corresponding to 100% efficiency. Such consideration for harmonic terminations was first introduced for over driven Class B by Snyder in 1967 [14]. The impedance termination conditions introduced by Snyder were implemented in Very High Frequency (VHF) band. For higher frequencies, the active device does not easily operate as a switch. In addition, implementation is not easily performed due to the drain capacitance, lead inductance, lead length (including bond wires), and dispersion (frequency-dependent propagation velocity) [15].

2.3 Waveform Engineering Based Approaches

If drain waveforms are assumed to be interchangeably square wave and half sine wave as shown in Fig.2.3, one has only even harmonics and the other has only odd harmonics; hence the product of harmonic current and voltage will be zero.

2.3.1 High Efficiency Class F / Inverse Class F

In class F design approach, drain voltage is assumed a square wave and drain current is assumed a half sine wave. Half sine current is set by biasing of the gate voltage. The resulting ideal drain voltage waveform is then a square wave as depicted in Fig.2.3.

Drain voltage has only odd harmonics and drain current has only even harmonics as expressed below:

\[
i_D(\theta) = \frac{I_{d,\text{peak}}}{\pi} + \frac{I_{d,\text{peak}}}{2}\sin(\theta) - \frac{2I_{d,\text{peak}}}{3\pi}\cos(2\theta) - \frac{2I_{d,\text{peak}}}{15\pi}\cos(4\theta) - \frac{2I_{d,\text{peak}}}{35\pi}\cos(6\theta) - \ldots
\]

\[
v_D(\theta) = \frac{V_{\text{max}}}{2} - \frac{2V_{\text{max}}}{\pi}\sin(\theta) - \frac{2V_{\text{max}}}{3\pi}\sin(3\theta) - \frac{2V_{\text{max}}}{5\pi}\sin(5\theta) - \frac{2V_{\text{max}}}{7\pi}\sin(7\theta) - \ldots
\]

So not only are drain waveforms non-overlapped, but also output power at harmonics is:
\[ \sum_{n=2}^{\infty} P_{out,nf} = V_{ds,2f}I_{d,2f} + V_{ds,3f}I_{d,3f} + V_{ds,4f}I_{d,4f} + V_{ds,5f}I_{d,5f} + \ldots \]  

\[ = 0 \times \frac{2I_{d,peak}}{3\pi} + \frac{2V_{max}}{3\pi} \times 0 + 0 \times \frac{2I_{d,peak}}{15\pi} + \frac{2V_{max}}{5\pi} \times 0 + \ldots = 0 \]  

Then, having square waveform for drain voltage and half sine wave for drain current result in theoretically 100% efficiency. To achieve this voltage, load impedance must be short at even harmonics and open at odd harmonics as below:

\[ Z_{n} = \begin{cases} 
0 & n, \text{even} \\
\infty & n, \text{odd} 
\end{cases} \]  

Such ideal conditions are not met in practical cases because the voltage waveform is formed by the current and load impedance. Practically, up to the third harmonics are con-
<table>
<thead>
<tr>
<th>Class F/Inverse F PAs</th>
<th>Frequency (GHz)</th>
<th>PAE (%)</th>
<th>Output Power (dBm)</th>
<th>Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[25] (2008)</td>
<td>2.45 / 3.3</td>
<td>53 / 46</td>
<td>33 / 32.5</td>
<td>8 / 6</td>
</tr>
<tr>
<td>[26] (2008)</td>
<td>1.7 / 2.14</td>
<td>31.5 / 50</td>
<td>32.8 / 34.4</td>
<td>5</td>
</tr>
<tr>
<td>[27] (2009)</td>
<td>3.5</td>
<td>78</td>
<td>40.4</td>
<td>12</td>
</tr>
<tr>
<td>[28] (2009)</td>
<td>2.45</td>
<td>71</td>
<td>39.4</td>
<td>14.4</td>
</tr>
<tr>
<td>[29] (2010)</td>
<td>2.15</td>
<td>84.9</td>
<td>39.1</td>
<td>18.4</td>
</tr>
<tr>
<td>[30] (2011)</td>
<td>0.8 / 1.25</td>
<td>81.7 / 80</td>
<td>40.6 / 41.8</td>
<td>14 / 15</td>
</tr>
</tbody>
</table>

**Table 2.1:** Performance comparison of Class F/inverse F PA designs

trollable considerably. Practical issues of controlling harmonics over third harmonic are described in [15].

Experimental implementations of the harmonic terminating for optimum behavior were investigated by several authors [16–18]. Regarding limitations imposed by the input and output non-linearities of the active device on the ideal class F condition, harmonic-generating mechanisms was investigated in [19]. It is shown that the third harmonic of the voltage must be of opposite phase with regard to the fundamental component in order to have a properly flat voltage waveform.

Inverse class F was proposed by [20] as the dual of the class F where the drain voltage is half sine and drain current is square wave as shown in Fig.2.3. A comparative analysis described in [21] shows that, under the same drain bias condition, the inverse class F amplifier has greater PAE than the class F amplifier when on-resistance of the transistor is taken into account. Recently, some other detailed investigations of modeling and design methodology of class F/inverse F power amplifier have been carried out in [22, 23].

**2.3.2 Discussion**

Harmonically tuned PA modes such as class F and inverse class F which are reviewed above rely on precise short and open harmonic terminations. Maintaining such specific fundamental and harmonic impedance lead to narrow band performance and theoretically limited achievable relative bandwidths. That is why most of the state-of-the-art PA perfor-
mances in this area are evaluated in a single frequency or dual band as reported in Table 2.1. Such trends were focused on bandwidth up to 5% or less due to tight spectrum allocation in wireless communications. Recent standards such as WiMAX and 4G required larger bandwidths up to 100 MHz. This motivated researchers to develop wide-band design techniques. The continuous mode PA design approach was then proposed which requires reactive second harmonic in order to extend achievable bandwidth.

2.3.3 Wide-band Continuous Mode Class J

To mitigate the problem of narrow band performance of class F and inverse class F amplifier, a continuous mode of operation was introduced by Cripps in [31]. If the overlapping pattern of drain voltage and current remains constant, it is interpreted as keeping the same efficiency. Recall the key mechanism of generating drain voltage by drain current and load termination. Similar to class B, drain current is considered half sine wave taking into account harmonics up to the second harmonic as below:

\[ i_D(\theta) = \frac{I_{\text{max}}}{\pi} + \frac{I_{\text{max}}}{2} \cos(\theta) + \frac{2I_{\text{max}}}{3\pi} \cos(2\theta) \]  \hspace{1cm} (2.14)

where \( \theta = \omega t \) and \( \omega = 2\pi f \). Including knee voltage of the transistor, which is shown in Fig.2.3 as \( V_K \) and is considered the voltage level after which drain current is saturated, a set of intrinsic drain voltage for class J is defined as below [32]:

\[ v_{DS}(\theta) = V_K + (V_{DC} - V_K)(1 - \cos\theta)(1 - \alpha\sin\theta) \]  \hspace{1cm} (2.15)

where \( \alpha \) parameter is varied over the range of \(-1 \leq \alpha \leq 1\). Then, the intrinsic fundamental and second harmonic load termination of the active device is obtained by dividing Eq.2.15 by Eq.2.14 as below [32]:

\[ Z_{f0} = \left. \frac{V}{(-T)} \right|_{f0} = \frac{(V_{DC} - V_K)(1 + j\alpha)}{I_{\text{max}}/2} = R_{\text{opt}} + j\alpha R_{\text{opt}} \]  \hspace{1cm} (2.16)
Figure 2.4: Fundamental and second harmonic load trajectories known as continuous mode design space (© 2013 IEEE [38])

\[
Z_{2f0} = \frac{\bar{V}}{(-\bar{I})}|_{2f0} = \frac{-(V_{DC} - V_K) j \alpha}{2 \left(\frac{2I_{max}}{3\pi}\right)} = -j\frac{3\pi}{8} \alpha R_{opt}
\]  \hspace{1cm} (2.17)

where \(\bar{V}\) and \(\bar{I}\) are the phasors of drain voltage and current respectively. \(-\bar{I}\) implies the opposite direction of the load current and drain current. \(R_{opt}\) is defined as below:

\[
R_{opt} = \frac{2(V_{DC} - V_K)}{I_{max}}
\]  \hspace{1cm} (2.18)

Fig. 2.4 shows such intrinsic load termination known as the design space over which efficiency, output power and gain is the same as those of class B [32].

Terminating intrinsic drain of the active device with such fundamental and second harmonic load results in a continuum of the drain voltage over variation of \(\alpha\) parameter as shown in Fig. 2.5.

As it can be seen, \(\alpha = 0\) corresponds to well known class B. As parameter \(\alpha\) varies, overlap of drain voltage and half sine drain current remain constant, leading to the same efficiency as for Class B over this range of variation. Early implementations of this theory was reported by [33, 34] exhibiting considerable improvement of bandwidth performance.
Figure 2.5: Theoretical drain voltage of class J over variation of $\alpha$ (© 2009 IEEE [31])

<table>
<thead>
<tr>
<th>Class J PAs</th>
<th>Bandwidth (GHz)</th>
<th>Bandwidth (%)</th>
<th>Drain Efficiency (%)</th>
<th>Output Power (dBm)</th>
<th>Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[33] (2009)</td>
<td>1.4 - 2.6</td>
<td>60</td>
<td>60 - 65</td>
<td>39 - 40</td>
<td>10 - 11</td>
</tr>
<tr>
<td>[39] (2010)</td>
<td>0.78 - 1</td>
<td>25</td>
<td>77 - 80</td>
<td>42 - 43</td>
<td>12 - 13</td>
</tr>
<tr>
<td>[40] (2011)</td>
<td>2 - 2.2</td>
<td>10</td>
<td>35 - 65</td>
<td>34 - 40</td>
<td>5 - 11</td>
</tr>
<tr>
<td>[36] (2011)</td>
<td>2.3 - 2.7</td>
<td>16</td>
<td>60 - 68</td>
<td>40</td>
<td>12 - 15</td>
</tr>
<tr>
<td>[41] (2012)</td>
<td>0.5 - 0.9</td>
<td>57</td>
<td>50 - 70</td>
<td>28 - 32</td>
<td>12 - 15</td>
</tr>
<tr>
<td>[42] (2012)</td>
<td>1.6 - 2.2</td>
<td>32</td>
<td>51 - 68</td>
<td>39 - 42</td>
<td>7 - 17</td>
</tr>
<tr>
<td>[43] (2013)</td>
<td>1.65 - 2.7</td>
<td>48</td>
<td>55 - 72</td>
<td>39 - 41</td>
<td>11 - 14</td>
</tr>
</tbody>
</table>

Table 2.2: Performance comparison of Class J PA designs

compared to previous high efficiency designs. As depicted in Table 2.2, continuous mode design space resulted in efficient performance across the extended range of frequency compared to Table 2.1.

Several investigations have been carried out based on class J design theory. Nonlinear effect of output capacitor of the active device in second harmonic behavior [35], wide-band harmonic suppression [36], GaAs MMIC based class J for X-band [37], integrated analysis and design of class J [32] and Class J design for Cognitive Radio [38] are some of the major attempts for different applications. Table 2.2 summarizes these results and some other designs of class J PA.
2.3.4 Discussion

It is important to note that class J theory, which is based on waveform engineering approach, confronts two issues.

First, waveform engineering in practical terms requires the investigation of intrinsic drain current and voltage in time domain. In other words, proposed trajectories must be applied to the intrinsic drain of the transistor, which is not easily accessible in discrete applications. There are two solutions to make sure that intrinsic waveforms are appropriately applied to the intrinsic drain: 1) complex and costly setup for monitoring intrinsic waveforms as reported in [44]. 2) extracting a non-linear, large signal and wide-band model for parasitic elements from intrinsic plane to external pin of the device. Otherwise monitoring of intrinsic waveforms can not go beyond simulation.

Second, theoretically, achievable bandwidth of class J approach is inherently limited to one octave. Design space concept of continuous mode operation is defined as the range of load terminations through which current and voltage waveforms keep the same overlapping pattern. Then efficiency and output power remain constant. This range, in class J, emanates from the theoretical expressions describing reactive fundamental and second harmonic impedances to be applied to intrinsic drain as described in Eq.2.16 and 2.17. As depicted in Fig.2.6, proposed reactive second harmonic corresponds to the edge of Smith chart.

Knowing that the second harmonic is out-of-band, we have:

\[ BW = f_2 - f_1 \]  \hspace{1cm} (2.19)

\[ f_2 < 2f_1 \] \hspace{1cm} (2.20)

\[ BW < f_1 \]  \hspace{1cm} (2.21)
It reveals that, from the theoretical point of view, there is an inherent limitation on bandwidth in continuous class J design space such that even if the gap between the first and second harmonic trajectories is somehow minimized, the bandwidth cannot exceed one octave. According to fractional bandwidth, it is limited to 66% as below:

$$\text{FractionalBW} = \frac{f_2 - f_1}{f_2 + f_1} = \frac{2f_1 - f_1}{2f_1 + f_1} = \frac{f_1}{3f_1} = 66\% \quad (2.22)$$

The results reported in Table 2.2 verify such inherent limitation of bandwidth performance. This limitation can be considerably mitigated if trajectories are defined based on characterized behavior of the active device, which is described in section 2.4.

### 2.4 Load-Pull Based Approaches

Under small signal or linear condition, device characterization of the power amplifier design procedure can be performed in terms of scattering parameters. However, as explained in section 2.2.2, high efficiency designs deal with harmonic tuning. Generating and control of harmonics are the result of non-linear behavior of the active device in higher input power levels or large signal condition.

The large signal performance of the active device plays a critical role in the power amplifier design. In particular, optimum design of the output and input matching networks...
Figure 2.7: Load-pull measurement setup

requires large signal characterization of the active device. In fact, scattering parameters are no longer effective in terms of device representation under non-linear conditions. Load-pull technique is then described as a non-linear tool for large signal device characterization [45].

2.4.1 Load-pull Measurement System

A load-pull setup consists of the device under test (DUT) with impedance tuners at the output (and input). The impedance tuners provide the DUT with the tunable load/source impedance while simultaneously measuring the DUT performance as shown in Fig. 2.7. The source impedance is mainly tuned to enhance the power gain of the active device. The large signal performance can be investigated as a function of input and output terminations, bias point and input power. The results can be then presented on the Smith chart in terms of efficiency and output power contour levels as depicted in Fig. 2.8. These contours are the loci of set of impedances over which amplifier exhibit constant output power or PAE.

2.4.2 Device Characterization Using Load-pull

Providing the designer with an accurate load impedance target, load-pull setup has been considered as a very good tool for RF power amplifier design for many years. Due to the recent development of fast nonlinear CAD tools, load-pull simulation alleviates the need for an expensive and multi-harmonic load-pull experimental setup. In other words, the load-
Figure 2.8: Load-pull contours (a) output power with 2dB steps (b) PAE with 10% steps
(© 2009 John Wiley [13])

pull process can be carried out with a commercial simulator using a nonlinear model for the
active device. The active device model provided by the manufacturers usually includes all parasitic elements from current generator plane to external pins of active device. Hence, deembedding of the parasitic elements are no longer of concern compared to the waveform engineering design approaches. This will largely simplify the design procedure. Using load-pull simulation, the active device can be characterized such that output power and efficiency contours are obtained. These contours provide the designer with load and source terminations for which maximum output power and efficiency are achieved.

The optimum performance in terms of the output power and efficiency can be characterized for each frequency. As a result, for each frequency, there is a load and source termination correspond to maximum achievable output power and efficiency. Consequently, input and output matching networks can be designed in order to present predicted impedance to input and output of the active device.
Table 2.3: Performance comparison of load-pull based PA designs

<table>
<thead>
<tr>
<th>wide-band PAs</th>
<th>Bandwidth GHz (%)</th>
<th>Drain Efficiency (%)</th>
<th>Output Power (%)</th>
<th>Gain (dBm)</th>
<th>CMPR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[46] (2008)</td>
<td>0.8 - 4 (133)</td>
<td>30 - 55</td>
<td>28 - 33</td>
<td>3 - 7</td>
<td>2 - 7</td>
</tr>
<tr>
<td>[48] (2010)</td>
<td>1.9 - 2.9 (42)</td>
<td>60 - 65</td>
<td>45 - 47</td>
<td>10 - 12</td>
<td>NA</td>
</tr>
<tr>
<td>[50] (2012)</td>
<td>0.9 - 1.5 (50)</td>
<td>45 - 60</td>
<td>42 - 44</td>
<td>13 - 15</td>
<td>5</td>
</tr>
</tbody>
</table>

2.4.3 Wide-band PA Design Using Load-pull Characterization

Several publications show the wide-band design of the PAs based on the load-pull analysis or measurements [46–50]. Most of these works are sub-octave and octave bandwidth as can be seen in Table 2.3. For an octave bandwidth, harmonics are out of band and they are optimized at the edge of Smith chart. For example, the octave bandwidth design proposed in [47] on the basis of the input and output characterization from 2 to 4 GHz as shown in Fig.2.9(a). wide-band PA design is then investigated by matching network design to apply characterized trajectory to the active device. Simulated impedance of the output matching network is shown in Fig.2.9(b). As it can be seen, the second harmonic from 4 - 8 GHz is optimized close to the edge of Smith chart.
2.4.4 Discussion

As mentioned in section 2.2.5, theoretically, the bandwidth of waveform engineering approaches is limited to one octave. This theoretical issue is not encountered when using load-pull characterization for wide-band design. Using both approaches, if the targeted bandwidth is octave or sub-octave, harmonics are optimized at the edge of Smith chart. Harmonics optimization becomes important particularly when the targeted bandwidth is larger than one octave. For instance, the multi-octave design proposed in [46] is a state-of-the-art design based on device characterization leading to optimized input and output impedance trajectories for 1-4 GHz depicted in Fig.2.10. Regarding the measured result of the implemented PA based on such trajectories as shown in Fig.2.11, there are some points worth noting.

Regarding small signal results shown in Fig.2.11, small signal gain, $S_{21}$, is reported 13 dB in the frequency range of 1 - 3.3 GHz. In this frequency range, the large signal gain is measured as 6-8 dB. It shows that large signal parameters including efficiency, output power and gain is measured in 5 - 7 dB compression point. Recall n dB compression point at which small signal gain is decreased by n dB. Regarding this level of saturation, measured drain efficiency in this range is 40% - 50%. This shows that multi-octave characterization of the active device has not led up to an optimum performance in the multi-octave range of 0.8 - 4.0 GHz. Degradation of the efficiency in the range of 1.5 - 2 GHz, for which the second harmonic is in-band, reveals that the second harmonic of this range may not be well optimized. Therefore, harmonic consideration for multi-octave PA design seems critical in final assessment of efficiency. In the next chapter, the impact of harmonic loads are investigated based on which a design methodology is proposed to design multi-octave PAs using load-pull characterization.
Figure 2.10: Multi-octave characterization reported by (© 2008 IEEE [46] )

Figure 2.11: (a) Small signal and (b) Large signal measurement results reported by (© 2008 IEEE [46] )
Chapter 3

Broadband RF Power Amplifier Design Methodology Using Sequential Harmonic Characterization

3.1 Introduction

As discussed in Chapter 2, wide-band approaches based on load-pull rely on the optimum loading of the actual active device. Using load-pull simulation or measurement, the transistor can be directly characterized. Load-pull simulation or measurement can be done for different frequencies to obtain optimum load impedance trajectories at the output terminal of the active device and the output matching networks can be designed directly for an octave bandwidth. Also, there is no theoretical limit on the bandwidth for load-pull based designs and a multi-octave design is practiced in [46]. However, any multi-octave approach inevitably implies dealing with in-band harmonics. Therefore, any load-pull approach for multi-octave performance requires in-band and out-of-band harmonics to be treated carefully, which is addressed in this chapter.

The objective of this chapter is to investigate the impact of in-band harmonics on the multi-octave performance of the PA. Then, a design methodology to effectively exploit in-band harmonics is presented. Introducing the sequential harmonic characterization, this methodology provides a more accurate impedance trajectory for multi-octave PA designs.

Since the proposed method is applied to the load-pull simulation, some initial steps such as the selection of RF power device, DC bias and stability analysis are carried out in advance. Then, the load-pull simulation setup is presented and followed by the investigation of the in-band harmonics effect when targeted bandwidth is larger than one octave. The sequential methodology is then presented and compared with the conventional load-pull. This comparison results in two different sets of trajectories, i.e. conventional trajectory and sequential trajectory. Consequently, two different output matching networks are designed for providing active device with these trajectories. Simulation results verify that a more
optimal performance can be achieved using the proposed technique. By using the proposed design technique, a broadband multi-octave power amplifier prototype is designed and fabricated using a Cree GaN HEMT device. The fabrication process for implementing the active device and thermal considerations are discussed. Experimental results verify multi-octave performance in terms of output power, efficiency, and gain over extended range of frequency.

### 3.2 RF Power Device Selection

RF high power device realization requires a proper selection of semiconductor materials to maintain desired levels of power and frequency performance while keeping heat transfer across the device and avoiding device failures. Particularly in commercial applications, RF power devices are mainly fabricated using III-V materials such as GaAs and GaN and IV materials such as silicon (Si) and germanium (Ge). Wide-bandgap materials such as Gallium Nitride (GaN) have been of great interest in research and development recently. Fig. 3.1 shows substrate properties such as energy bandgap, breakdown field, thermal conductivity and conductivity, which are more important in RF power devices [13].

The band-gap energy as the required energy for transferring an electron from the valence to conduction bands in a semiconductor is related to the maximum allowed temperature in the device and its power capabilities. A wider band-gap leads to higher power density, i.e. higher output power in smaller size. Output power density of 10-12 W/mm for GaN HEMT (High Electron Mobility Transistor) is reported [51]. Higher power density also requires dissipated heat in the device to be transferred without degrading performance due to increasing temperature. Hence, the thermal conductivity matters. Moreover, a higher avalanche field corresponds to the breakdown voltage allowing the device to operate at higher output voltages. Fig.3.2 and 3.3 report output power levels and efficiency versus frequency using different solid state materials for power amplifier design. Compared to Si and GaAs, GaN has lower electron/hole mobility. However, higher power density provides
higher output impedance closer to center of Smith chart that requires less quality factor for output matching networks. This leads to wider bandwidth suitable for broadband PA design [32].

GaN has superior properties compared to silicon (Si) or Gallium Arsenide (GaAs), including higher band-gap energy, higher breakdown voltage, and higher thermal conductiv-
It makes GaN technology a very good candidate for high power and wide-band power amplifier. Having said that, CGH60008D bare die device which is a Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) from Cree Inc. is selected for the wide-band power amplifier design. According to [52], this device has the following features:

- 15 dB Typical Small Signal Gain at 4 GHz.
- 12 dB Typical Small Signal Gain at 6 GHz.
- 8 W Typical $P_{sat}$ @ 28 V Operation.
- 5 W Typical $P_{sat}$ @ 20 V Operation.
- High Breakdown Voltage.
- High Temperature Operation.

That makes this device suitable for applications including broadband amplifiers and cellular infrastructures working at OFDM, W-CDMA, EDGE, CDMA and LTE waveforms.

### 3.3 PA Design and Simulation

The CGH60008D device model provided by manufacturer Cree is used for the PA design and simulation. The design and simulation are done using Advanced Design System (ADS)
3.3.1 DC Bias Point

In order to fairly compare the designed amplifier using the proposed method with other reported studies, including waveform engineering based class J, the bias point is selected as the same as in those studies, which is deeply class AB. Regarding negative pinch off voltage of the FET, gate voltage is swept from -4 to 1 while keeping drain voltage at 28 V as the operating drain voltage of this device. DC simulation setup and resulted IV curves is shown in Fig.3.4 and 3.5 respectively. The corresponding bias point is set on $V_{GS} = -3V$ and $I_D = 42mA$.

3.3.2 Stability

Stability is an important design criteria that should be considered in the amplifier design. In two-port systems, oscillations may occur when input or output resistance ports are negative. This negative resistance corresponds to input and output reflection coefficient greater than unity. K factor determines stability condition which is calculated using a set of S parameters at the working frequency defined as below:
\[ k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \]  

(3.1)

\[ \Delta = S_{11}S_{22} - S_{12}S_{21} \]  

(3.2)

Stability factor should be greater than one to guarantee stable performance in working frequencies. Fig.3.6 shows the simulated transistor is potentially unstable for some values of load and source reflection coefficients corresponding to \( k < 1 \) for a considerable portion of the bandwidth and presents a high gain at these frequencies as shown in Fig.3.7.
For making this transistor unconditionally stable, a parallel RC circuit is placed in the input of transistor shown in Fig.3.8. This circuit attenuates lower frequencies such that the transistor exhibits overall lower gain in these frequencies resulting in the stable condition shown in Fig.3.10. This stabilizer circuit pushes unstable regions of load and source reflection coefficients to the outside of Smith chart as shown in Fig.3.9.

### 3.3.3 Load-pull Simulation Setup

The load-pull simulation is performed using the Harmonic Balance tool with a non-linear and large signal model of the active device provided by manufacturer as shown in Fig.3.11. These contours are the loci of set of impedances over which the amplifier exhibits constant output power or PAE. Biasing and stability components are simulated using real models.

For drain inductance a CCI_0603CS series from Coilcraft is used, having features including ultra-small size, high Q and high Self Resonance Frequency (SRF) that makes them suitable for high frequency applications. Stability and input DC blocking capacitors are selected from multi-layer 100A series from ATC, which offers high Q, low Equivalent Series Resistance (ESR) and high Self Resonance Frequency (SRF).
3.4 In-band Harmonic Investigation

As discussed in section 2.3.2, for sub-octave and octave designs, harmonics are out of band and device characterization is performed using conventional load-pull. Conventional load-pull implies active device characterization where in-band harmonic is not the case. Then, device characterization at each frequency is independently performed through iterative fundamental and harmonic load-pull assuming harmonics at each frequency are set at the edge of Smith chart for optimized performance. This assumption emanates from theoretical harmonic manipulation described in section 2.2.2.

Recall that in class F and inverse F intrinsic drain is terminated to open and short interchangeably at second and third harmonics. However, intrinsic drain is not accessible
Figure 3.9: Load (dotted) and source (solid) stability circles for stabilized circuit

Figure 3.10: (a) Stability factor k and (b) Maximum gain vs. frequency for stabilized circuit in load-pull characterization. Passive parasitic elements cause the optimum impedances at package reference plane to be different from open and short loads.

As an example, load-pull simulations are performed for the sample frequency of $f_1 = 2$ GHz. The active device is biased at deep class AB with a drain voltage of 28 V and current of 42 mA. Fig.3.12 load-pull contours for output power and PAE as a function of load impedance. Fig.3.12(a) depicts output power and PAE lines resulted from second harmonic load-pull at $f_1 = 2$ GHz. This second harmonic load-pull is done by fixing the fundamental and input power. Fig.3.12(b) shows output power and PAE contours resulted
Figure 3.11: Load-pull simulation setup using active device model

from fundamental load-pull at $f_1 = 2$ GHz while second harmonic is set at the edge of Smith chart accordingly. In other words, fundamental impedance is located based on the optimized second harmonic. Maximum output power and PAE correspond to the innermost contours. The other contours are shown with $\%$ 2 and 0.2 dBm decrements for PAE and output power respectively.

It is important to mention that this procedure is no longer the optimum solution if the targeted bandwidth is larger than one octave such that second harmonics of some frequencies are in-band. For instance if the targeted bandwidth is assumed 1 GHz - 4 GHz, second harmonic of 2 GHz is in-band. Then, harmonic characterization should be modified for multi-octave designs. Having said that, device characterization at $f_1 = 2$ GHz requires $f_2 = 2f_1 = 4$ GHz to be optimized in advance.

Therefore, load-pull at $f_2 = 4$ GHz is performed in advance. Since $2f_2 = 8$ GHz as the second harmonic is beyond the targeted bandwidth, it is reasonable to be optimized at the edge of Smith chart. Resulting output power and PAE contours for the fundamental
Figure 3.12: Output power (solid blue) and PAE (dashed red) contours of (a) second harmonic and (b) fundamental conventional load-pull at 2 GHz

Figure 3.13: Output power (solid blue) and PAE (dashed red) contours of (a) second harmonic and (b) fundamental load-pull at 4 GHz

and harmonic load-pull at frequency of $f_2 = 4$ GHz are shown in Fig.3.13. Next, device characterization at $f_1 = 2$ GHz is modified based on the results at $f_2 = 2f_1 = 4$ GHz. In other words, $f_2 = 4$ GHz is an in-band harmonic and affects the fundamental load-pull at $f_1 = 2$ GHz as shown in Fig.3.14.

Comparison of two methods illustrates how second harmonic affects fundamental load optimization at $f_1 = 2$ GHz. Fig.3.15 compares PAE contours of fundamental load optimization shown in Fig.3.12 and Fig.3.14.
Conventional load-pull for fundamental load at $f_1 = 2$ GHz is performed setting the second harmonic at $Z_{2f,\text{con}} = 0.4+j1.8\Omega$ as obtained in harmonic load-pull of Fig.3.12(a). As it can be seen, fundamental load at 2 GHz located in $Z_{f,\text{con}} = 41+j5\Omega$ results in maximum PAE of 64.8 % using conventional load-pull. In contrast, having a targeted bandwidth larger than one octave, fundamental load-pull at $f_1 = 2$ GHz requires its second harmonic, $2f_1 = 4$ GHz, to be taken into account in advance. Fundamental load-pull at $f_1 = 2$ GHz is then performed, setting the second harmonic at $Z_{2f,\text{seq}} = 26+j30\Omega$ as obtained in fundamental load-pull at $2f_1 = 4$ GHz in Fig.3.13(b). PAE contours of the fundamental load-pull at 2 GHz is shown in 3.15 and $Z_{f,\text{seq}} = 72+j26\Omega$ corresponds to maximum PAE of 65.7 %. It is worth noting that $Z_{f,\text{con}}$ obtained in the conventional load-pull corresponds to 58.2 % on sequential contours. In other words, ignoring in-band harmonics causes sub-optimum design and performance degradation. Having said that, the sequential methodology for device characterization of multi-octave PA design is presented in the next section.
Consider a target bandwidth of $BW = f_{\text{stop}} - f_{\text{start}}$, where $f_{\text{start}}$ is the lowest design frequency and $f_{\text{stop}}$ is the highest design frequency. When the target bandwidth is greater than one octave, we have: $f_{\text{stop}} > 2f_{\text{start}}$. We designate the “lower in-band” frequency range as:

$$f_{\text{start}} < f_{\text{LIB}} < \frac{f_{\text{stop}}}{2}$$

In this frequency range, the second harmonics are inside the bandwidth. Also we use “higher in-band” term as:

$$\frac{f_{\text{stop}}}{2} < f_{\text{HIB}} < f_{\text{stop}}$$

For the higher in-band frequency range, the harmonic frequencies are out of the frequency band of interest. In the load-pull characterization, usually the harmonic impedances are set to obtain optimum performance in terms of output power or efficiency. However, for multi-octave design, the harmonic impedances of lower in-band frequencies cannot be selected.
arbitrarily since they are fundamental load impedances for the higher in-band frequencies. Consequently, the lower in-band frequencies cannot be characterized until their harmonics are located through load-pull for the higher in-band frequencies. Hence, the sequential harmonic characterization procedure for multi-octave designs is proposed as below:

1) Fundamental and harmonic load-pull for higher in-band frequencies are performed such that their harmonics are set at the edge of Smith chart for optimum performance.

2) These optimum fundamental load impedances obtained for higher in-band frequencies are set as harmonic load impedances of the load-pull for lower in-band frequencies to obtain the optimum load impedances at fundamental frequencies for the lower in-band frequencies. Fig.3.16 summarizes this procedure in a flowchart.
Hence, optimum reflection coefficients corresponding to maximum efficiency and output power are obtained sequentially for out-of-band, higher in-band, and lower in-band frequencies respectively leading to a more accurate characterization of the active device. It should be noted that if the harmonic load impedances are considered as reactive loads on the edge of Smith chart for all frequency points, then for lower in-band frequencies the obtained load trajectory will be different from the optimum load impedance due to the effect of the harmonic loading. This may cause sub-optimum performance and lead to a discrepancy between final amplifier’s performance and the results obtained by load-pull.

3.6 Sequential vs. Conventional Trajectories

Next step is device characterization for the multi-octave bandwidth of 0.75 - 4 GHz. The fundamental load impedances are selected at the intersection of 39 dBm output power contours and the highest possible efficiency. The proposed sequential method is compared to the conventional load-pull in the frequency band. Conventional method implies device characterization when all harmonic load impedances are considered at the edge of Smith chart.

Using the proposed technique, higher in-band frequencies (4, 3 GHz) are first found setting out-of-band harmonics (8, 6 GHz) at the edge of Smith chart. Similar fundamental load-pull simulation is then performed for lower in-band frequencies (2, 1.5 GHz) by setting their second harmonics (4, 3 GHz) at prelocated higher in-band. Consequently, fundamental loads at 1 GHz and 0.75 GHz are obtained by setting their second harmonic as found earlier.

As shown in Fig.3.17, targeted bandwidth is addressed differently in the two procedures. Higher in-band frequencies are located in the same area using either case, because they are found by the same out-of-band harmonic loads. However, lower in-band load impedances (e.g. 0.75, 1, 1.5, 2 GHz) differ when using proposed method confirming the effect of in-band harmonic. In fact, when targeted bandwidth is larger than one octave,
in-band harmonics of lower in-band frequencies are not purely reactive and must be found in advance by load-pull for the higher in-band frequencies.

3.6.1 Matching Network Design

After transistor characterization, performance investigation is then continued by design of matching networks to provide the active device with both trajectories. However, it is now more challenging as it has to cover harmonic load impedances over an extended range of frequency. Synthesizing matching network can be done using lumped elements or distributed lines. Moreover, investigation of the trajectories in PA performance requires matching network to accurately follow the trajectory, not only over targeted bandwidth but also out of band harmonics. Then, tolerance and Self Resonance Frequency (SRF) of lumped elements at RF frequencies are the main drawbacks toward this end. However, a distributed solution seems more flexible for RF broadband design.

Based on this, two matching networks for providing the active device with the conventional and sequential trajectories are designed using micro strip lines with substrate specifications of 812 um thickness and dielectric constant of 3.38 corresponding to Rogers

**Figure 3.17:** Active device characterization using sequential harmonic method in blue (Δ) and conventional load-pull in red (∇)
RO4003 laminates. Fig. 3.18 shows these two matching networks optimized to follow trajectories depicted in Fig. 3.19. As it can be seen, red dotted and blue dashed trajectories follow conventional and sequential trajectories respectively.

### 3.6.2 Simulation Results: Output Power and Efficiency Performance

After characterizing active device using conventional and sequential load-pull methods followed by matching network design corresponding to either trajectories, wide-band PA de-
sign is continued by applying input and output matching networks to the active device. Input matching network is optimized regarding input impedance of the active device through load-pull simulation using either methods considering conjugate match condition. Since active device used in this design is bare die, it is required to be connected to the input and output parts through wire bond as shown in Fig.3.20. Inductance $L_b$ represents wire bond connected to drain, gate and source.

Fig.3.21 shows output power and drain efficiency versus frequency of simulated wide-band PA using conventional and sequential trajectories when fed by CW input power. As it can be seen, either method results in wide-band performance in terms of output power, efficiency and gain for the multi-octave range of 0.5 - 4 GHz due to wide-band load-pull characterization shown in Fig.3.21. Sequential characterization gives output power of 39 - 40 dBm in the range of 0.5-3.5 GHz and drain efficiency greater than $\%$ 60 in the range of 0.6 - 4.0 GHz. Given constant input power of 28 dBm, large signal gain is 11 - 12 dB in the range of 0.5 - 3.8 GHz. On the other hand, designing PA with the output matching network corresponding to conventional trajectories results in almost the same output power while efficiency is degraded up to 12 $\%$ for lower in-band frequencies.

As mentioned in section 3.5, the main difference between the sequential and the conventional method relates to lower in-band frequencies. Having design bandwidth larger than one octave puts higher in-band frequencies to higher priority in characterization procedure. Then, fundamental loads at lower in-band frequencies are not optimized until their harmonics, which are fundamental loads at higher in-band frequencies. Otherwise, lower in-bands are addressed in sub-optimum characterization. It is worth noting that proper application of characterized load is ensured, based on how accurate matching network follows optimized trajectory over the whole range of frequencies. Fig.3.22 demonstrates PA performance in terms of output power, efficiency and gain while input power is swept from 0 - 30 dBm and frequency is set at 1, 2, 3 and 4 GHz.
Figure 3.20: Schematic of simulated wide-band PA using sequential load-pull
3.7 Broadband PA Fabrication and Measurement

The broadband power amplifier design based on sequential harmonic characterization is pursued by realizing simulated PA. Thermal calculation is the first step of realization process following by device implementation. Measurement setup and wide-band calibration are then presented. Finally, experimental results of PA realization is demonstrated in terms of promised wide-band performance.

3.7.1 Thermal Calculation

Since the CGH60008D active device used in this design is a bare die, thermal consideration becomes very important to ensure proper performance of the PA. As mentioned in section 3.2, RF devices made of GaN materials benefit from high power density i.e. higher generated power in a small area increasing operating temperature. Some part of this power is delivered to the output and the rest is dissipated in the device generating heat. This heat must be transferred properly; otherwise, junction temperature exceeds maximum rating and device structure breaks down. With this in mind, thermal calculation is necessary prior to
Heat generated in a bare die device is transferred by using an epoxy adhesive with enough thermal conductivity. Then, thermal calculation requires determining the minimum thermal conductivity of the epoxy to ensure the dissipated power in the device is transferred properly, while delivering expected RF output power to the load. Thermal conductivity is estimated based on the conductive heat transfer expressed by Fourier’s Law \[ q = \frac{kA\Delta T}{S} \] as:

where \( q \) is transferred heat \( (W/L_s) \), \( A \) is heat transfer area, \( k \) is thermal conductivity of the material, \( \Delta T \) is temperature difference across the material and \( S \) is material thickness. According to CGH60008D data sheet [52], the area through which heat should be transferred is identical to the die dimension which is 820\( \mu m \times 920\mu m \) depicted in Fig.3.23. Material thickness is the summation of the thickness of the transistor [52] and epoxy which
is 150µm. Also, dissipated power to be transferred is calculated based on efficiency and RF output power. Assuming average efficiency of 60% and output power of 8 W, dissipated power is estimated as:

\[ P_{\text{diss}} = P_{\text{DC}} - P_{\text{out}} = P_{\text{out}} \left( \frac{1}{\eta} - 1 \right) = 8 \left( \frac{1}{0.6} - 1 \right) = 5.3 \text{W} \]  

(3.6)

Then, we have:

\[ k\Delta T = \frac{qS}{A} = \frac{5.3 \times 150\mu m}{820\mu m \times 920\mu m} = 1053 \frac{W}{m} \]  

(3.7)

According to the data sheet [52], maximum operating junction temperature is 225°C. Assuming room temperature of 25°C, maximum temperature difference will be \( \Delta T = 200 \). Then we have:

\[ k_{\text{min}} = \frac{1053}{200} = 5.26 \frac{W}{mK} \]  

(3.8)

It reveals that in order to keep the device working, i.e. junction temperature remains below the maximum rating, the epoxy adhesive used as heat transferring material should have minimum thermal conductance of 5.26 \( \frac{W}{mK} \). Based on this, DIEMAT DM6030Hk with thermal conductivity of 60 \( \frac{W}{mK} \) is used to attach bare die to the aluminum plate for heat transfer. For this thermal calculation, it has been assumed that thermal variation of the plate is negligible and only the step experiences a considerable temperature variation.

### 3.7.2 Device Implementation

After thermal calculation, an aluminum plate is designed in AutoCAD and manufactured. Die device is mounted and attached to a step made in the center of the plate as shown in Fig.3.24. Attachment of the die to plate is carried out based on the curing profile recommended in DM6030Hk datasheet [54] as shown in Fig.3.25. This profile is loaded into the programmable oven to bake the epoxy and have die stuck to the step on the plate.
the baking process, the die device is well attached to the step on the plate through epoxy. All drain, gate, and source pads are wire bonded to the PCB for electrical connection as depicted in Fig. 3.26. The power amplifier including input and output matching, stability circuit, biasing components and decoupling capacitors are implemented on Rogers RO4003 substrate with 0.032 inch thickness and dielectric constant of 3.38 as simulated in section 3.5.1. The PCB dimension is $42\text{mm} \times 34\text{mm}$. The photograph of the amplifier and the transistor chip area are shown in Fig. 3.26.

**Figure 3.23:** Overall size of CGH60008D [52]

**Figure 3.24:** Design of plate in AutoCAD covered with PA layout extracted from ADS (left), Manufactured aluminum plate (right)
3.7.3 Measurement Setup and Calibration

The implemented PA is evaluated by large-signal measurement to demonstrate wide-band performance. Measurement setup consists of Agilent E8247C CW signal generator, AR 5S1G4 driver, an isolator, a 30 dB attenuator, coupler, Anritsu MS2665C spectrum analyzer and Boonton 3400 RF power meter as indicated in Fig. 3.27. Large signal measurement is done using CW signal generated by signal generator and boosted by driver to provide...
designed PA with adequate input power. Also, the isolator placed between driver and PA avoids any probable high power reflections and protects the signal generator and driver from back reflection. To cover the whole frequency range, two isolators are used; one working in 1-2 GHz and the other in 2-4 GHz. High power output signal of the PA is attenuated by 30 dB and followed by a coupler feeding spectrum analyzer and power meter. Regarding high output power of PA, 30 dB attenuator is used to restrain the power from exceeding levels high enough to damage the spectrum analyzer and power meter. Spectrum analyzer is monitored for any case of instability.

Prior to performance measurement, it is necessary to calibrate setup components including RF cables, driver, attenuator, coupler and isolators for the whole range of frequency. For this end, signal generator, power supplies, spectrum analyzer and power meter are connected through General Purpose Interface Bus (GPIB) cables and controlled by the aid of MATLAB. Calibration implies how input power from signal generator and measured power at power meter should be translated to input and output power of the PA respectively. In other words, how much power should be sent from signal generator to have desired level of
Figure 3.28: Schematic of calibration and measurement setup

Figure 3.29: Measurement results of the realized PA at 1 GHz

power in the input of PA and how much power from power meter should be de-embedded to calculate output power of the PA. This is done by determining total loss across cables, isolators, attenuator, and coupler in addition to actual gain and output power of the driver. Then, extracted S2P files are de-embedded by means of MATLAB. Finally, main PA parameters such as output power, gain and efficiency are calculated and plotted in MATLAB.
3.7.4 Experimental Results

wide-band measurement requires wide-band calibration. Hence, this calibration procedure described in section 3.6.3 must be carried out for the whole targeted bandwidth. Calibration was performed at the frequency intervals of 100 MHz. After calibrating the setup over
Figure 3.32: Measurement results of the realized PA at 4 GHz

the whole bandwidth, power sweep measurements were performed at different frequencies with frequency spacing of 100 MHz. Fig.3.29, 3.30, 3.31, and 3.32 indicate measured performance of realized PA in terms of output power, gain, PAE and drain efficiency versus input power at frequencies of 1, 2, 3, and 4 GHz plotted in MATLAB. Drain current and voltage are also measured and plotted in following figures.

PA performance in terms of frequency swept from 0.7 - 4.0 GHz with 100 MHz increment is depicted in Fig.3.33. All measured and simulated parameters of Fig.3.33 are obtained at 3dB gain compression compared to the small-signal gain. 3 dB compression point is the input power level at which small signal gain is decreased by 3 dB. A drain efficiency of 53 - 64 % is obtained over frequency range of 0.7 – 4.0 GHz which is equivalent to the fractional bandwidth of 140 %. At 3 dB gain compression, the amplifier’s output power is attained in the range of 37.5 - 39.1 dBm.

As shown, a reasonable agreement between measurement and simulation results are noted. Table 3.1 compares the performance of this work with other wide-band GaN HEMT PAs. The designed prototype based on our proposed characterization technique exhibits larger fractional bandwidth compared to other experiments including waveform shaping approaches [32,33,55] and octave bandwidth using conventional load-pull characterization
Figure 3.33: Measurement and simulation results of realized PA in terms of drain efficiency, output power and gain versus frequency

<table>
<thead>
<tr>
<th>wide-band PAs</th>
<th>BW GHz (%)</th>
<th>η (%)</th>
<th>$P_{sat}$ (dBm)</th>
<th>Saturated Gain (dB)</th>
<th>CMPR (dB)</th>
<th>Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>[46] (2008)</td>
<td>0.8 - 4 (133)</td>
<td>30 - 55</td>
<td>28 - 33</td>
<td>3 - 8</td>
<td>2 - 7</td>
<td>Die</td>
</tr>
<tr>
<td>[33] (2009)</td>
<td>1.4 - 2.6 (60)</td>
<td>60 - 65</td>
<td>~ 40</td>
<td>~ 10</td>
<td>2</td>
<td>Package</td>
</tr>
<tr>
<td>[47] (2010)</td>
<td>1.9 – 4.3 (78)</td>
<td>57 - 72</td>
<td>40 – 42</td>
<td>9 – 11.5</td>
<td>NA</td>
<td>Die</td>
</tr>
<tr>
<td>[32] (2013)</td>
<td>2.25 – 3.08 (30)</td>
<td>50 - 58</td>
<td>24 - 27</td>
<td>6 - 10</td>
<td>3.2</td>
<td>MMIC</td>
</tr>
<tr>
<td>[55] (2014)</td>
<td>1 - 3 (100)</td>
<td>57 - 67</td>
<td>39 - 41.5</td>
<td>10 - 12.2</td>
<td>NA</td>
<td>Package</td>
</tr>
<tr>
<td>[56] (2014)</td>
<td>1.5 - 5.5 (114)</td>
<td>50 - 57</td>
<td>43-44</td>
<td>7 - 10</td>
<td>NA</td>
<td>Die</td>
</tr>
<tr>
<td>This Work</td>
<td>0.7 - 4 (140)</td>
<td>53 - 64</td>
<td>37.5 – 39.1</td>
<td>6 - 13</td>
<td>3</td>
<td>Die</td>
</tr>
</tbody>
</table>

Table 3.1: Performance comparison of the realized PA with other wide-band GaN PAs

[47]. Also, higher efficiency and higher large signal gain is obtained at lower compression point compared to the multi-octave PA reported in [46].
Chapter 4

Conclusion and Future Work

4.1 Conclusion

In this thesis, the necessity of the wide-band and high efficiency design of the RF power amplifier was studied. High efficient design reduces dissipated heat and enhances the device’s lifetime. Moreover, reduction of interference and better spectrum management, efficient usage of bandwidth and power, seamless portability and evolution, and longer lifetime for terminals have made SDR and cognitive radio architectures promising solutions for multi-standards and multi-band operations. These radio architectures appreciate wide-band design to mitigate hardware replacement costs. wide-band and high efficiency design techniques were then reviewed based on waveform engineering approach and device characterization method.

Waveform engineering Class J offers efficient performance over an extended range of frequency compared to classic high efficiency class F/inverse F techniques. However, it suffers from theoretical limitation of bandwidth up to one octave. On the other hand, this limitation is not of concern in device characterization methods using load-pull; however, multi-octave design requires in-band harmonics to be dealt with accordingly.

For multi-octave designs, load impedances at in-band harmonic frequencies have a considerable impact on the PA performance. Based on the sequential load-pull characterization technique proposed in this thesis, load impedances at higher in-band frequencies should be considered prior to lower in-bands. Otherwise, sub-optimum performance such as degradation of efficiency will be inevitable. Sequential harmonic characterization was then proposed to take into account harmonics across the whole targeted bandwidth effectively, thus, leading to more accurate characterization of load impedances at lower in-band frequencies.

Thanks to higher power density and frequency performance, wide-band PA design is pursued using a device model of GaN HEMT bare die provided by CREE. Simulation
results of the designed PA verified that using sequential trajectory leads to higher efficiency up to 12% at in-band frequencies compared to the conventional trajectory. A prototype PA was then fabricated and realized on RO4003 laminate. Experimental results demonstrated broadband efficiency of 53% - 64% at 3-dB compression point across 0.7 – 4 GHz, which is equivalent to 140% fractional bandwidth.

4.2 Discussion and Future Work

The sequential method proposed in this thesis has been practiced with emphasis on second harmonic effect according to relative importance. Passive and active device models are not accurate at the third harmonic of higher in-band frequencies. However, harmonic characterization can be investigated theoretically up to n-th harmonic as a general case of sequential method as further steps. Regarding this end, it should be noted that higher priority is given to the frequencies with out of band harmonic. In other words, assume a k-octave targeted bandwidth of $BW = f_{stop} - f_{start}$. Then, if $n$ is the highest order of harmonic to be taken into account, highest priority in load-pull for device characterization is given to following range, which has out of band n-th harmonic:

$$\frac{2^k f_{start}}{n} < f_n < f_{stop}$$

(4.1)

Therefore, n-th harmonic load-pull for this range should be done in advance. Consequently, n-th harmonic of this range is the m-th harmonic of following range:

$$\frac{2^k f_{start}}{m} < f_m < \frac{n f_{stop}}{m}$$

(4.2)

Then, fundamental load-pull of $f_m$ should be done by setting $f_n$ range as m-th harmonic of this load-pull. Because practically up to the third harmonic are feasible to manipulate, applying sequential load-pull to the third harmonic in the presence of the second harmonic and implementation of the designated PA for experimental investigation would be a good
extension of this work.

Furthermore, increasing bandwidth of modulated signals has been recently considered to enhance network capacity. For instance, Long Term Evolution (LTE)-advanced as a 4G wireless communication standard utilizes signal bandwidth of up to 100 MHz. High peak to average power ratio (PAPR) of this signal requires PA to operate in large back-off, leading to efficiency degradation. Then, load modulation networks are employed to keep efficiency in back-off levels. Asymmetrical transistors used in load modulation limit the instantaneous bandwidth of the PA [57], thus, making wide-band design in this area of a concern. Therefore, device characterization based on proposed sequential method can be considered as a potential wide-band PA design approach for load modulation regime.
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